IN THE CLAIMS:

Please amend the claims as follows:

1. (currently amended) A thin film transistor array panel comprising:

an insulating substrate;

a plurality of ~~first signal~~ gate lines formed on the insulating substrate;

a plurality of ~~second~~ data ~~signal~~ lines insulated from the ~~first signal~~ gate lines and intersecting the ~~first signal~~ gate lines; and

a plurality of groups, each group comprising:

a pair ~~plurality~~ of first and second pixel electrodes capacitively coupled to each other, disposed on pixel areas defined by intersections of the ~~first signal~~ gate lines and the ~~second signal~~ data lines and arranged in a matrix;

a ~~plurality of~~ first thin film transistor~~s, each having three terminals~~ connected to one of the ~~first signal~~ gate lines~~,~~ and one of the ~~second signal~~ data lines, and connected to or capacitively coupled to ~~one of~~ the first pixel electrode~~s~~; and

~~a plurality of second pixel electrodes disposed on the pixel areas and capacitively coupled to the first pixel electrodes; and~~

a ~~plurality of~~ second thin film transistor~~s, each having a terminal~~ connected to ~~one of~~ the second pixel electrode~~s~~ and ~~another terminal connected to~~ one of the ~~first signal~~ gate lines that is ~~connected~~ disconnected from the first thin film transistor~~to one of the firs pixel electrodes in a pixel area in an adjacent row~~.

2. (currently amended) The thin film transistor array panel of claim 1, wherein each group further comprises ~~comprising~~ a ~~plurality of~~ coupling electrode~~s that are~~ connected to or overlapping the first pixel electrode~~s~~ and overlap the second pixel electrode~~s~~ with being insulating therefrom.

3. (currently amended) The thin film transistor array panel of claim 2, wherein the coupling electrode~~s~~ is ~~are~~ connected to a drain electrode~~s~~ of the first thin film transistor~~s connected to the first pixel electrodes~~.

4. (currently amended) The thin film transistor array panel of claim 1, further comprising a plurality of ~~third~~ signal lines intersecting the ~~second signal~~ data lines, wherein ~~a final terminal of each of~~ the second thin film transistor~~s~~ is connected to one of the ~~third~~ signal lines and the ~~second signal~~ data lines.

5. (currently amended) The thin film transistor array panel of claim 4, wherein ~~the~~

~~final terminal of each of~~ the second thin film transistor~~s~~ is connected to one of the ~~third~~ signal lines, and ~~the~~ each group ~~thin film transistor array panel~~ further comprises a ~~plurality of~~ third thin film transistor~~s~~, ~~each having three terminal~~ connected to one of the ~~second signal~~ data lines, ~~one of~~ the second pixel electrode~~s~~, and one of the gate ~~first signal~~ lines connected to the second thin film transistor~~a pixel area in an adjacent row~~.

6. (currently amended) The thin film transistor array panel of claim 1, wherein at least one of the first pixel electrode~~s~~ and the second pixel electrode~~s~~ comprises at least one domain partitioning member.

7. (currently amended) The thin film transistor array panel of claim 2, further comprising:

a gate insulating layer disposed between the ~~first signal~~ gate lines and the ~~second signal~~ data lines; and

a passivation layer disposed between the ~~second signal~~ data lines and the first and the second pixel electrodes,

wherein the coupling electrode~~s~~ is ~~are~~ connected to the first pixel electrode~~s~~ through a contract hole~~s~~ at the passivation layer.

8. (original) A liquid crystal display comprising:

a first insulating substrate;

a gate line formed on the first insulating substrate and including first and second gate electrodes;

a storage electrode line formed on the first insulating substrate;

a gate insulating layer covering the gate line and the storage electrode line;

first and second amorphous silicon layers formed on the gate insulating layer;

a data line formed on the gate insulating layer and including a first source electrode disposed on the first amorphous silicon layer at least in part;

a second source electrode disposed on the second amorphous silicon layer at least in part;

first and second drain electrodes formed on the first and the second amorphous silicon layers at least in part and disposed opposite the first and the second source electrodes, respectively;

a coupling electrode formed on the gate insulating layer;

a passivation layer formed on the data line, the first and the second drain electrodes, and the coupling electrode;

a first pixel electrode that is formed on the passivation layer and is connected to or

overlaps the first drain electrode and the coupling electrode;

a second pixel electrode insulating from the first pixel electrode, connected to or overlaps the first drain electrode and the coupling electrode;

a second insulating layer facing the first insulating substrate; and

a common electrode formed on the second insulating substrate.

9. (original) The liquid crystal display of claim 8, wherein the second source electrode is connected to the storage electrode line or the data line.

10. (original) The liquid crystal display of claim 9, wherein the second source electrode is connected to the storage electrode line, and the liquid crystal display further comprises a third gate electrode connected to the gate line, a third source electrode connected to the data line, and the third drain electrode connected to the second pixel electrode.

11. (original) The liquid crystal display of claim 9 or 10, wherein the first drain electrode is connected to the coupling electrode.

12. (original) The liquid crystal display of claim 9, wherein the coupling electrode is connected to the first pixel electrode through a contact hole at the passivation layer.

13. (original) The liquid crystal display of claim 9, further comprising:

a first domain partitioning member disposed on at least one of the first and the second substrates; and

a first domain partitioning member disposed on at least one of the first and the second substrates and partitioning a pixel area into a plurality of domains along with the first domain partitioning member.